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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/020,647	Fjelstad
Examiner	**Group Art Unit**
David E. Graybill	2814

☒ Responsive to communication(s) filed on *12 Nov 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-11 and 21-34* is/are pending in the applicat

Of the above, claim(s) *24* is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-11, 21-23, and 25-34* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3,4 and 5*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Claims 4, 6, 28 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 4 and 28 there is insufficient literal antecedent basis for the term "the exposed surface of the bond ribbons."

In claim 6 there is insufficient literal antecedent basis for the term "the terminal positions."

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwon (5070297).

Kwon teaches:

1. A method of creating a compliant semiconductor chip package assembly comprising the steps of providing a first dielectric protective layer 34 on a contact bearing surface of a semiconductor chip 14, wherein the semiconductor chip has a central region bounded by chip contacts 36 of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures such that the chip contacts are exposed; providing a compliant layer 32 atop the first dielectric protective layer within the central region, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges

between the top surface and the bottom surface; and selectively electroplating bond ribbons 28 atop the first dielectric protective layer and the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal 20-22-24 on the top surface of the compliant layer.

2. The method according to Claim 1 further including the step of providing a second dielectric protective layer 26 atop exposed assembly elements 28 on the terminal side of the assembly after the step of selectively electroplating the bond ribbons, wherein the second dielectric protective layer has a plurality of apertures such that the terminals are exposed.

3. The method according to Claim 1 wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

4. The method according to Claim 1 further including the step of providing for an encapsulant layer 26 atop the exposed surface of the bond ribbons.

6. The method according to Claim 4 further including the step of providing for a second dielectric protective layer 21 atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures such that the terminal positions are exposed.

7. The method according to Claim 1 wherein a silicon dioxide passivation layer on the face surface of the semiconductor chip comprises the first dielectric protective layer.

11. The method according to Claim 1 wherein the sloping edges of the compliant layer have a first transition region near the top surface of the compliant layer and a second transition region near

the bottom surface of the compliant layer and wherein both the first transition region and the second transition region have a radius of curvature.

21. A method of making a compliant microelectronic assembly comprising the steps of: providing a microelectronic element 38 having a first surface and a plurality of contacts 36 disposed on the first surface thereof; providing a compliant layer 32 over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more edge surfaces extending between said top and bottom surfaces, and then selectively forming flexible bond ribbons 28 over said compliant layer so that said bond ribbons extend over said top surface and one or more of said edge surfaces and said bond ribbons electrically connect said contacts to conductive terminals 20-22-24 overlying the top surface of said compliant layer.

22. The method as claimed in claim 21, wherein said contacts on said microelectronic element are disposed in a first region of said first surface, said compliant layer overlies a second region of said first surface, and one or more edge surfaces include one or more border edge surfaces extending along one or more borders between said first and second regions.

23. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

25. The method as claimed in claim 21, further comprising the step of: before the providing a compliant layer step, providing a first dielectric protective layer 34 on the first surface of the microelectronic element, the first dielectric layer having a plurality of apertures therein so that said

contacts are accessible therethrough, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

26. The method as claimed in claim 25, the selectively forming flexible bond ribbons step including selectively electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

27. The method as claimed in claim 21, further including the step of providing a dielectric cover layer 21 over said compliant layer and said bond ribbons after the step of selectively forming the bond ribbons, wherein the cover layer has a plurality of apertures so that said terminals are accessible therethrough.

28. The method as claimed in claim 21, further including the step of providing an encapsulant layer 26 over the exposed surface of the bond ribbons.

29. The method as claimed in claim 28, further including the step of providing a second dielectric protective layer 21 atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures so that said terminals are accessible therethrough.

30. The method as claimed in claim 21, further including the step of depositing a barrier metal 30 atop said contacts, prior to the step of forming the bond ribbons, whereby the barrier metal (inherently) helps to prevent voiding between the contacts and the bond ribbons.

33. The method as claimed in claim 21, wherein the edge surfaces of the compliant layer are sloping surfaces which extend in both vertical and horizontal directions.

34. The method as claimed in claim 33, wherein at least some of said sloping edge surfaces have first transition regions near the top surface of the compliant layer and second transition regions

near the bottom surface of the compliant layer, and wherein both the first and second transition regions have respective radii of curvature.

Although Kwon does not appear to explicitly teach a process wherein both the first and second transition regions have respective radii of curvature, this property is inherent in the process of Kwon.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (5070297).

Kwon is applied as it was applied to claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34.

As cited supra, Kwon teaches:

8. The method according to Claim 1 further including the step of plating a barrier metal 30 atop the semiconductor chip contacts, whereby the barrier metal (inherently) helps to prevent voiding at the boundary between the semiconductor chip contacts and the bond ribbons. However, Kwon does not appear to explicitly teach the practice of this step prior to the step of providing the compliant layer. Nonetheless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise

critical. In fact, there is no support for this claim limitation elsewhere in the disclosure. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. *Ex parte Rubin 128 USPQ (PO BdPatApp 1959).*

Kwon also does not appear to explicitly teach:

5. The method according to Claim 4 wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel. Nonetheless, as cited, Kwon teaches that "Protective coating 26 may comprise any number of compliant materials having sufficient elastic, protective, and adhesive properties for the purposes of the present invention." Furthermore, judicial notice is taken that it is well known to select protective coating encapsulant layers from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel. Moreover, it would have been obvious to combine the well known process with the process of Kwon because it would provide a protective coating.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon as applied to claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34 supra, and further in combination with Palagonia (5874782).

As cited supra, Kwon teaches:

9. The method according to Claim 1 applied simultaneously to a multiplicity of undiced semiconductor chips 14 on a wafer 10 to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

10. The method according to Claim 1 applied simultaneously to a multiplicity of adjacent semiconductor chips 14 arranged in an array to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

31. The method as claimed in claim 21, the method being applied to a plurality of undiced semiconductor chips 14 on a wafer 10 to form a corresponding plurality 12 of compliant semiconductor chip packages 14.

32. The method as claimed in claim 21, the method being applied to a plurality of adjacent semiconductor chips 14 arranged in an array to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

However, Kwon does not appear to explicitly teach:

9. The method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

10. The method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

31. The method further including the step of separating the packages following the step of depositing the bond ribbons.

32. The method further including the step of separating the packages following the step of selectively electroplating the bond ribbons.

Nevertheless, Palagonia teaches a method including a step of dicing and separating a plurality of adjacent compliant semiconductor chip packages 22 arranged in an array on a wafer 20 following a step of selectively electroplating bond ribbons 26. Moreover, it would have been obvious to combine the process of Palagonia with the process of Kwon because it would facilitate testing of individual chips.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist at (703) 308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m..

The fax phone number for group 2800 is (703)305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.